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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/788,560	01/24/1997	SHUNPEI YAMAZAKI	0756-1626	7940

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ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 08/788,560	Applicant(s) YAMAZAKI ET AL.	
	Examiner ori nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *78-157* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *78-157* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *14,16* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 78-101, 110-115, 117-127, 129-138 and 146-157 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. (4,755,865) in view of Saito et al. (4,772,927) and Shizukuishi et al. (4,841,348).

Wilson et al. teach in figure 3 substantially the entire claimed structure, including a MOS transistor comprising a silicon semiconductor layer 42 comprising a channel region 42B in contact with source and drain regions 42A, 42C at a source/drain-channel boundary, a gate electrode 44 adjacent the channel region with gate insulating film 43 interposed therebetween, and a region 42C formed in the semiconductor layer containing one or more elements selected from a group consisting of carbon, nitrogen and oxygen at a concentration higher than 10E15 atoms per cm cube or more (column 4, lines 39-49), wherein the region is formed in the vicinity of at least one of the source/drain-channel boundary, and one boundary of the region is located within at

least one of the source region and the drain region, and wherein the channel region containing boron (column 6, lines 31-32).

Although Wilson et al. do not explicitly disclose one boundary of the region being located within the channel region, this feature is inherent in Wilson et al.'s device for the following reasons. First, Wilson et al. teach in figure 3 a region 42C having one boundary located within at least one of the source region and the drain region, and the other boundary located at the boundary between the channel region and the source/drain region. The boundary between the channel region and the source/drain region is the location where dopant atoms of the source and drain regions cease to be present. The area where dopant atoms are present is the source/drain region and the area where dopant atoms are not present is the channel region. Since the region inhibits grain boundary migration of dopant atoms, dopant atoms will terminate within the region (Note that this is the intended use of the region in Wilson et al.'s invention). Therefore, a portion of the region wherein dopant atoms of the source and drain regions are not present is located within the channel region Thus, Wilson et al. teach one boundary of the region being located within the channel region, and not aligned with edges of the gate electrode, as claimed. Second, Wilson et al. teach in figure 3 a region 42C having one boundary located at the boundary between the channel region and the source/drain region, wherein "the implanted oxygen or nitrogen [the region] .....does not migrate significantly" (column 4, lines 56-59). This means that some

migration of oxygen or nitrogen occurs. Since the region has one boundary located at the boundary between the channel region and the source/drain region, even minute migration means that the one boundary would be located within the channel region, and not aligned with edges of the gate electrode, as claimed.

Wilson et al. do not teach a display device having a plurality of pixels and at least one driver circuit for driving the pixels, wherein the carbon, nitrogen and oxygen are at a concentration of 10E19 atoms per cm cube or more

Shizukuishi et al. teach a MOS transistor being used in a CMOS device which is part of a peripheral circuit of an active matrix type device having plurality of pixels (abstract), and formed of a semiconductor film comprising amorphous silicon (column 3, line 48). Note that a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). In this case, using a MOS transistor in a CMOS device, and using the CMOS device as a driver, stagger, inverted stagger, planar and inverted planar type transistors in a peripheral circuit of an active matrix display device having plurality of pixels is a recitation of the intended use of a structure which does not add to the structural limitations in the body of the claim

Furthermore, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Therefore, the claimed structure is considered to be in at least obvious over the Wilson et al.'s structure.

Saito et al. teach a MOS transistor in figure 1e comprising a semiconductor film comprising crystalline silicon (column 1, lines 19-20) and a channel region 7 in between source and drain regions 6, a gate electrode 9 adjacent the channel region with gate insulating film 5 interposed therebetween, wherein the source and drain regions have at least one portion containing one or more elements selected from a group consisting of carbon, nitrogen and oxygen at a concentration of 10E19 atoms per cm cube or more (column 3, line 49 to column 4, line 24), formed in a CMOS device (figure 2).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Wilson et al.'s transistor in a CMOS device which is part of a peripheral circuit of an active matrix type device having plurality of pixels, wherein the carbon, nitrogen and oxygen are at a concentration of 10E19 atoms per cm cube or more because it is conventional in the art to connect individual transistors in order to

form a CMOS device, and it is well known in the art to use CMOS transistors as drivers in a peripheral circuit of an active matrix type device having plurality of pixels. It is also well within the skills of an artisan to use carbon, nitrogen and oxygen at a concentration of 10E19 atoms per cm cube or more. The combination is motivated by the teachings of Saito et al. who point out the advantages of using a TFT transistor having source and drain regions containing carbon, nitrogen or oxygen at a concentration higher than 10E19 atoms per cm cube or more in a CMOS device.

Regarding claim 84, the claimed limitations of a region having higher energy band gap than any of the source, drain and channel regions is inherent in Wilson et al.'s device, because a region having elements selected from a group consisting of carbon, nitrogen and oxygen, has higher energy band gap than a region containing boron.

Regarding claims 90, 96, 105, 111, 119, 127, 134, 140, 147 and 153, although Wilson et al. do not explicitly disclose a channel region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm cube, Wilson et al. teach diffusing impurities at concentration of from 10E15 to 5X10E17 atoms per cm cube (column 6, lines 36-37), and under certain processing conditions the channel region can have similar concentration (column 6, lines 64-66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a channel

region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm in Wilson et al.'s device, since adjusting the amount of impurity concentration in a semiconductor device is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization. Saito et al. teach a channel region having at least one portion containing one or more elements selected from a group consisting of carbon, nitrogen and oxygen at a concentration higher than 10E19 atoms per cm cube or more (column 5, lines 20-23).

Regarding claim 134, Wilson et al. teach that the oxygen migrates into the channel region (column 4, lines 56-59). Therefore, one boundary of the region is formed in the channel region and the other boundary is formed in one of the source/drain regions.

Regarding claims 83, 95, 125, 133, the claimed limitations of an element concentration in the channel region being lower than that of the element in the region is inherent in Wilson et al.'s device, because the concentration of a region naturally tends to be higher at the center and lower at the periphery of the region.

3. Claim 116 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al., Saito et al. and Shizukuishi et al., as applied above, and further in view of Solheim (5,219,784).

Wilson et al. and Saito et al. teach substantially the entire claimed structure, as above, except a threshold voltage of an NMOS being approximately equivalent to that of the PMOS.

Solheim teaches a threshold voltage of an NMOS being approximately equivalent to that of the PMOS (column 4, lines 45-55).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use of a threshold voltage of an NMOS being approximately equivalent to that of the PMOS in Wilson et al. and Saito et al.'s device, since adjusting the threshold voltage is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization, depending on the intended use of the device.

4. Claims 128 and 139 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. and Saito et al., as applied to claims 102, 110, 118, 126 above, and further in view of Higashi et al. (4,694,317).

Wilson et al. and Saito et al. teach substantially the entire claimed structure, including a first interlayer insulating film (ILD) 10 (Saito et al.) comprising inorganic material, and a gate electrode comprising a silicon film containing phosphorus (Wilson et al., column 3, lines 38-40, and column 6, line 32). Wilson et al. and Saito et al. do not teach a

second ILD film comprising organic resin and a pixel electrode on the second ILD film formed in a transparent or a reflective device.

Higashi et al. teach in figure 1D a transparent or a reflective device comprising a first interlayer insulating film 5 comprising inorganic material, a second ILD film 7 comprising organic resin and a pixel electrode 11 on the second ILD film (column 3, line 64 to column 4, line 48).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second ILD film comprising organic resin under a pixel electrode in Wilson et al.'s device, in order to provide better protection for the device. The combination is motivated by the teachings of Higashi et al. who point out the advantages of using an organic ILD film under a pixel electrode in a TFT transistor.

5. Claims 102-107, 109 and 140-144 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al., Saito et al. and Shizukuishi et al., as applied above, and further in view of Ovshinsky et al. (4,766,471).

Wilson et al., Saito et al. and Shizukuishi et al. teach substantially the entire claimed structure, as applied above, except an element comprising carbon.

Ovshinsky et al. teach elements selected from a group consisting of carbon, nitrogen and oxygen, can widen the band gap in silicon layer containing elements such as germanium or boron. It would have been obvious to a person of ordinary skill in the art

at the time the invention was made to use an element comprising carbon in Wilson et al., Saito et al. and Shizukuishi et al.'s device, in order to widen the energy band gap of the device. Note that substitution of materials is not patentable even when the substitution is new and useful. Safetran Systems Corp. v. Federal Sign & Signal Corp. (DC NIII, 1981) 215 USPQ 979.

Regarding claim 105, although Wilson et al. do not explicitly disclose a channel region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm cube, Wilson et al. teach diffusing impurities at concentration of from 10E15 to 5X10E17 atoms per cm cube (column 6, lines 36-37), and under certain processing conditions the channel region can have similar concentration (column 6, lines 64-66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a channel region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm in Wilson et al.'s device, since adjusting the amount of impurity concentration in a semiconductor device is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

6. Claim 145 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al., as applied above, and further in view of Higashi et al. (4,694,317).

Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al. teach substantially the entire claimed structure, including a first interlayer insulating film (ILD) 10 (Saito et al.) comprising inorganic material, and a gate electrode comprising a silicon film containing phosphorus (Wilson et al., column 3, lines 38-40, and column 6, line 32). Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al. do not teach a second ILD film comprising organic resin and a pixel electrode on the second ILD film formed in a transparent or a reflective device.

Higashi et al. teach in figure 1D a transparent or a reflective device comprising a first interlayer insulating film 5 comprising inorganic material, a second ILD film 7 comprising organic resin and a pixel electrode 11 on the second ILD film (column 3, line 64 to column 4, line 48).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second ILD film comprising organic resin under a pixel electrode in the device of Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al., in order to provide better protection for the device. The combination is motivated by the teachings of Higashi et al. who point out the advantages of using an organic ILD film under a pixel electrode in a TFT transistor.

7. Claim 108 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al., as applied above, and further in view of Solheim (5,219,784).

Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al. teach substantially the entire claimed structure, as above, except a threshold voltage of an NMOS being approximately equivalent to that of the PMOS.

Solheim teaches a threshold voltage of an NMOS being approximately equivalent to that of the PMOS (column 4, lines 45-55).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use of a threshold voltage of an NMOS being approximately equivalent to that of the PMOS in the device of Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al., since adjusting the threshold voltage is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization, depending on the intended use of the device.

Response to Arguments

8. Applicant argues that Wilson et al. do not teach one boundary of the region being located within the channel region and not aligned with edges of the gate electrode.

First, Wilson et al. teach in figure 3 a region 42C having one boundary located within at least one of the source region and the drain region, and the other boundary located at the boundary between the channel region and the source/drain region. The boundary between the channel region and the source/drain region is the location where dopant atoms of the source and drain regions cease to be present. The area where dopant atoms are present is the source/drain region and the area where dopant atoms are not present is the channel region. Since the region inhibits grain boundary migration of dopnat atoms, dopant atoms will terminate within the region (Note that this is the intended use of the region in Wilson et al.'s invention). Therefore, a portion of the region wherein dopant atoms of the source and drain regions are not present is located within the channel region. Thus, Wilson et al. teach one boundary of the region being located within the channel region, as claimed. Second, Wilson et al. teach in figure 3 a region 42C having one boundary located at the boundary between the channel region and the source/drain region, wherein "the implanted oxygen or nitrogen [the region] .....does not migrate significantly" (column 4, lines 56-59). This means that some migration of oxygen or nitrogen occurs. Since the region has one boundary located at the boundary between the channel region and the source/drain region, even minute migration means that the one boundary would be located within the channel region and not aligned with edges of the gate electrode. Therefore, although

figure 3 depicts a boundray aligned with edges of the gate electrode, the actual boundary is not aligned with edges of the gate electrode.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
December 23, 2002

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800